

FIG.1

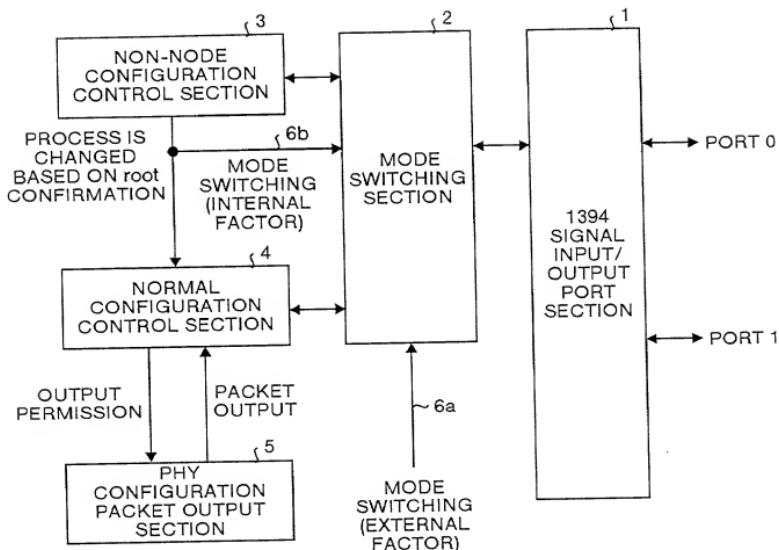


FIG.2

12		11		10		9		8		7		6		5		4		3		2		1		0	
00	phy_ID	R	T	gap_count	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

LOGICAL INVERSION OF FIRST Quad let

FIG.3

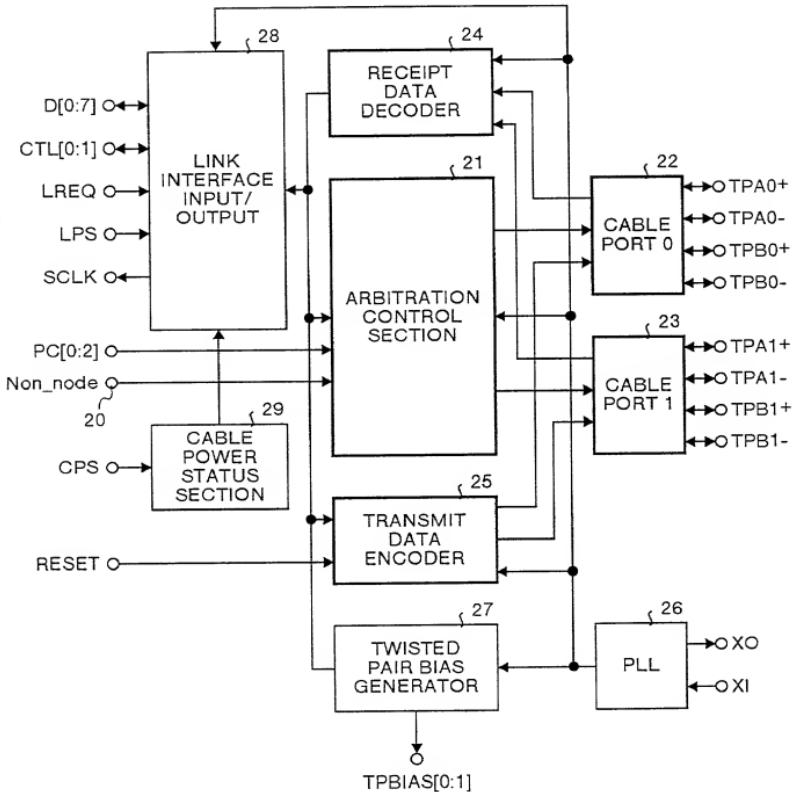


FIG. 4

NAME OF TERMINALS	I/O	FUNCTION
TPA0+	I/O	FIRST PORT TWISTED PAIR CABLE A POSITIVE PHASE INPUT/OUTPUT
TPA0-	I/O	FIRST PORT TWISTED PAIR CABLE A NEGATIVE PHASE INPUT/OUTPUT
TPB0+	I/O	FIRST PORT TWISTED PAIR CABLE B POSITIVE PHASE INPUT/OUTPUT
TPB0-	I/O	FIRST PORT TWISTED PAIR CABLE B NEGATIVE PHASE INPUT/OUTPUT
TPA1+	I/O	SECOND PORT TWISTED PAIR CABLE A POSITIVE PHASE INPUT/OUTPUT
TPA1-	I/O	SECOND PORT TWISTED PAIR CABLE A NEGATIVE PHASE INPUT/OUTPUT
TPB1+	I/O	SECOND PORT TWISTED PAIR CABLE B POSITIVE PHASE INPUT/OUTPUT
TPB1-	I/O	SECOND PORT TWISTED PAIR CABLE B NEGATIVE PHASE INPUT/OUTPUT
XI	-	LIQUID CRYSTAL OSCILLATOR CONNECTION TERMINAL
XO	-	LIQUID CRYSTAL OSCILLATOR CONNECTION TERMINAL
TPBIAS0	O	FIRST PORT-USE TWISTED PAIR BIAS OUTPUT
TPBIAS1	O	SECOND PORT-USE TWISTED PAIR BIAS OUTPUT
D[7:0]	I/O	LINK INTERFACE DATA INPUT/OUTPUT
CTL[0:1]	I/O	LINK INTERFACE CONTROL INPUT/OUTPUT
LREQ	I	LINK REQUEST INPUT
LPS	I	LINK POWER STATUS INPUT
SCLK	O	LINK CONTROL-USE CLOCK OUTPUT
PCI[0:2]	I	POWER CLASS SETTING (SEE IEEE Std 1394-1995, SECTION 4.3.4.1)
Non-node	I	NON-NODE/NORMAL MODE SETTING INPUT
CPS	I	CABLE POWER STATUS INPUT
RESET	I	RESET INPUT

FIG.5

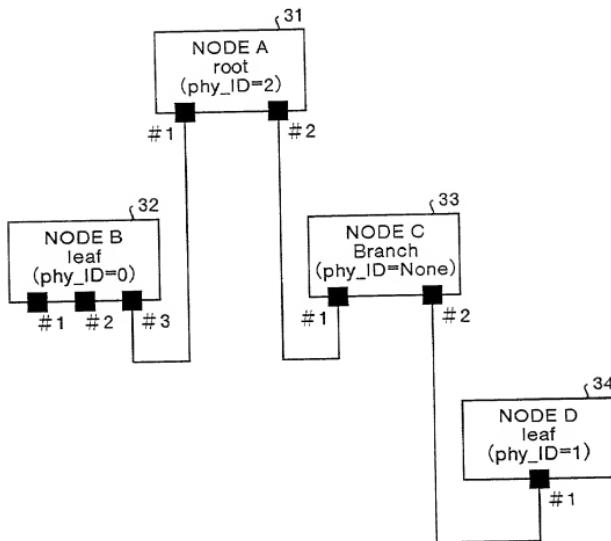


FIG.6

